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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/695,624	10/28/2003	Ulf Tohsche	INFN/0033	6423

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EXAMINER	
NGUYEN, LONG T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 03/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/695,624	TOHSCHE, ULF	
	Examiner	Art Unit	
	Long Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-8,10,11 and 15-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-4,6-8,10 and 11* is/are allowed.

6)☒ Claim(s) *15-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 February 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 15-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claim 15, this claim is indefinite because there is no connection or structural relationship between "a single data input" and other elements in the circuit, i.e., the "single data input" recited on line 2 of the claim is floating.

Claims 16-20 are indefinite because they include the indefiniteness of claim 15.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 15, 16, 19 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Ichioka et al. (JP 2-210907).

Insofar as understood in claims 15-16, Figure 7 of the Ichioka et al. reference discloses a flip-flop which includes: a single data input (the terminal for receiving signal D); a clock signal (CK); a data signal (D); a non-inverted output (Q); and inverted output (Q/); a first holding element (51B, 52) having first (N41) and second (N42) nodes; and a second holding element (81,

82B) having third (N62) and fourth (N61) nodes. Note that when clock CK goes Hi (first edge), then the first node (N41) having the logic value of the data signal (D) while the second node (N42) having the logic level of inverted logic value of the data signal (i.e., D/); and when clock CK goes Lo (second edge), then the logic value (D) at the first node (N41) is transferred to the non-inverted output node (Q) via the fourth node (N61), and the inverted logic value (i.e., D/) of the data signal (D) at the second node (N42) is transferred to the inverted output node (Q/) via the third node (N62). Note, it is seen in the operation of the flip-flop in Figure 7 that a propagation delay of the non-inverted logic level from the first node (N41) to the non-inverted output node (Q) is substantially equal to a propagation delay of the inverted logic level from the second node (N42) to the inverted output node (Q/), i.e., each propagation delay = 2 inverters and 1 pass gate; and the first and second feedback loops each comprises reset circuitry (NOR gate 52 for the first feedback loop, and NOR gate 81 of second feedback loop) responsive to reset signal to the place the inverted and non-inverted output nodes at known logic levels regardless of the state of the clock signal (CK). Note that, the reset circuitry of the first feedback loop (i.e., NOR 52) comprises a NOR gate (52) having a first input coupled to R, a second input coupled to the second node N42, and an output coupled to the first node (N41).

Insofar as understood in claim 19, it is seen in Figure 7 that a first signal path between the first node (N41) and the non-inverted output node (Q) and a second signal path between the second node (N42) and the inverted output node (Q/) each comprises the same number of circuit elements (2 inverters and 1 pass gate).

Insofar as understood in claim 20, Figure 7 shows the first and second signal paths each comprises two inverters (61 and 91 for the first path, and 62 and 92 for the second path).

5. Claims 15-17 19 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Robertson et al. (US 2002/0005745 A1).

Insofar as understood in claims 15-16, Figure 11 of the Robertson et al. reference discloses a flip-flop which includes: a single data input (the terminal for receiving signal D); a clock signal (CLK); a data signal (D); a non-inverted output (Q); and inverted output (QZ); a first holding element (39) having first (output of inverter 28) and second (input of inverter 28) nodes; and a second holding element (41) having third (input of inverter 31) and fourth (output of inverter 31) nodes. Note that when clock CLK goes Lo (first edge), then the first node having the logic value of the data signal (D) while the second node having the logic level of inverted logic value of the data signal (i.e., D/); and when clock CLK goes Hi (second edge), then the logic value (D) at the first node is transferred to the non-inverted output node (Q) via the fourth node, and the inverted logic value (i.e., D/) of the data signal (D) at the second node (N42) is transferred to the inverted output node (QZ) via the third node. Note, it is seen in the operation of the flip-flop in Figure 11 that a propagation delay of the non-inverted logic level from the first node to the non-inverted output node (Q) is substantially equal to a propagation delay of the inverted logic level from the second node to the inverted output node (QZ), i.e., each propagation delay = 2 inverters and 1 pass gate; and the first and second feedback loops each comprises reset circuitry (NOR gate 40 for the first feedback loop, and NAND gate 42 of second feedback loop) responsive to reset signal (PREZ) to the place the inverted and non-inverted output nodes at known logic levels regardless of the state of the clock signal (CLK). Note that, the reset circuitry of the first feedback loop (i.e., NOR 40) comprises a NOR gate (40) having a first input

coupled to signal PRE, a second input coupled to the second node (by way of inverter 28) and an output coupled to the first node (by way of inverter 28).

Insofar as understood in claim 17, Figure 11 shows the reset circuitry (NAND 42) of the second feedback loop (41) comprises one gate (42) controlled by the clock signal (CLK) and responsive to the reset signal (PREZ).

Insofar as understood in claim 19, it is seen in Figure 11 that a first signal path between the first node (output of 28) and the non-inverted output node (Q) and a second signal path between the second node (input of 28) and the inverted output node (QZ) each comprises the same number of circuit elements (2 inverters and 1 pass gate).

Insofar as understood in claim 20, Figure 11 shows the first and second signal paths each comprises two inverters (31 and 14 for the first path, and 28 and 25 for the second path).

Allowable Subject Matter

6. Claims 1-4, 6-8, 10 and 11 are presently allowed.

7. Claim 18 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, and if amended to overcome the informalities and/or the rejection under 35 U.S.C. 112, 2nd paragraph set forth above.

Response to Arguments

8. Applicant's arguments filed on 11/28/05 have been considered but are not persuasive.

Applicant argues that Ichioka does not discloses a resettable flip-flop comprising a single data input as Figures 7 of Ichioka has inputs D and D-bar. However, this argument is not persuasive because Ichioka discloses a single data input (the terminal for receiving signal D).

Note that terminal for receiving signal D-bar is another single data input. Also, it is note that the claims and the specification do not specifically recited that the flip-flop consisting only a single data input (i.e., no where in the claims and the specification recites any specific recitation that prevents the flip-flop from having another input), so for broadest reasonable interpretation, the terminal for receiving signal D is reasonable to be considered as "single data input", and thus Ichioka meets all the limitations of claim 15.

Applicant also argues that Robertson et al. does not disclose a resettable flip-flop comprising a single data input because Figure 11 shows data inputs D and SD. However, this argument is not persuasive because Robertson et al. discloses a single data input (the terminal for receiving signal D). Note that terminal for receiving signal SD is another single data input. Also, it is note that the claims and the specification do not specifically recited that the flip-flop consisting only a single data input (i.e., no where in the claims and the specification recites any specific recitation that prevents the flip-flop from having another input), so for broadest reasonable interpretation, the terminal for receiving signal D is reasonable to be considered as "single data input", and thus Robertson et al. meets all the limitations of claim 15.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Thursday from 8:00am to 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LONG NGUYEN
PRIMARY EXAMINER